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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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23389 7590 03/14/2008 SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA SUITE 300 GARDEN CITY, NY 11530			EXAMINER PADGETT, MARIANNE L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/674,648	Applicant(s) CHOE ET AL.	
	Examiner MARIANNE L. PADGETT	Art Unit 1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 9/17/2007, 12/5/2007 & 12/06/2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14, 16-24, 26-36 and 39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14, 16-24, 26-36, 39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. Applicant submission of terminal disclaimer (TD) over SN 10/674,647 submitted on 12/5/2007, has been approved, hence overcomes the provisional obviousness double patenting (ODP) rejection with respect to that case in section 8 of the action mailed 6/15/2007, however it is noted that all three TD's submitted on 9/17/2007 indicated that they were with respect wrong application number (10/647,648), instead of the present case's application number of 10/674,648, thus were **not** effective TD's for overcoming ODP rejections over PN 6,486,037 or 6,800,578.

Applicants' amendment to paragraph [0048] has appropriately corrected inconsistencies therein with respect to the figure's reference numbers to which they referred, which were objected to in section 2 of the action mailed 6/15/2007.

2. Claims **1-14, 16-24, 26-36 & 39** are rejected under 35 U.S.C. **112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants have stated that they have integrated the subject matter of claim 15 into independent claim 1, however this is incorrect., since as amended independent claim 1 requires the "first porosity region" (\equiv upper layer) to have a greater density (i.e. less porosity (assuming in line 6 of claim 1, "that" should be --than--)), & the "second porosity region" to have a lower density or be less dense (i.e. greater porosity), but original claim 15 required the "upper region of less dense porous Si and a lower region of more dense porous Si", which is just the opposite of what is now explicitly claimed. It is further noted, that while paragraph [0014] has teachings concerning "Upon... oxidation step, the fine buried porous layer is converted into a buried oxide, while the course top layer coalesces into a solid Si-containing over-layer by migration of Si atoms", where the fine layer was disclosed as under the course layer, this only gives support for the " coalesces " & "solid" language, not the claimed densities, as [0014] only gives relative size relationship for the pores in the top (= top = first) & buried (= lower = second) layers, where the

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examiner notes that pore size does not necessitate either greater or lower density, as it does not define the distribution or number of pores, which are also factors which determine the density or its inverse porosity of a material. Although, it is noted that frequently a material with larger pore sizes is less dense or more porous than a material with smaller pore sizes, this is not a necessary or inherent relationship, hence cannot be assumed & would not support the amendment anyhow. With respect to paragraph [0048] which is describing figure 1, specifically reference numbers found in 1C & 1D, that was amended in the response (9/17/07 & 12/6/07) for consistency within the paragraph & with the figures, clearly have the fine pore region at the bottom of the overall porous region & having a lower number of pores, thus being more dense & lower porosity, hence the top part of the porous region having the coarser pores, has by comparison more pores, with higher porosity (more porous) or less dense (lower density). Paragraph [0058] cited by applicants & the abstract have teachings equivalent to [0014] for purposes of amended claim 1. For these reasons, applicants' claims as amended are directed to **New Matter**, which is explicitly contrary & opposite to the teachings founded the body of the specification & figures. While the examiner suspects that applicants have accidentally turned around or mixed up their nomenclature, the examination must be based on what they have actually claimed.

Applicants' amendment has only incorporated some of the limitations from claim 2 into the independent claim, particularly it is no longer required to supply the dopant to the dopant region via ion implantation in any of the claims, although claims 5 & 6 require their specific dopants to be "implanted", however not necessarily as ions as **previously** required by claim 2 from which claims 5 & 6 depend. Since disclosures in the specification concerning forming the dopant region, when these materials & parameters are employed, require ion implantation ([0037-39]), this broadening the scope encompasses **New Matter**. Furthermore, the original claims 31-34 & disclosure ([0022] & [0040]) concerning the contradictively named "neutral ion", requires it to be used in a dual ion implantation process, i.e. used in conjunction with ion implanting dopant, hence this limitation, which also previously depended from the

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requirement of ion implantation, encompasses more **New Matter**. (Although note that implanting a **single** ion or atom as required by claims 31-32 & 34, could hardly have any significant effect on the entire substrate, as one ion (or atom) is all that is required by these claims). It is noted that the independent claim can technically be considered to be supported for "providing a dopant region" via means other than ion implantation, if one considers the entire substrate to be the dopant region, as it is taught that the "Si-containing substrate may be undoped, or doped." ([0035]), except there is no disclosure that such a generically doped substrate would produce the claimed two different porosity regions, or if the claimed porosity regions were consistent with the disclosure or original claim 15, that a generically (uniformly) doped substrate would produce the taught 2 porosity regions, thus this context also appears to encompass **New Matter**. Also note that the original claims & the disclosures that require a dopant region to be being formed, disclosed that it is done by implanting or ion implantation ([0020] & [0037]), thus delineating the scope required to avoid introducing new matter. Further note that the original annealing limitations/steps related to activating the ion implanted dopant & annealing disclosures in the specification ([0042-46]) analogously relate to formed dopant region 12, thus required ion implantation to be used & the claims relating thereto now also encompass **New Matter**.

With respect claim 7, applicants have **broadened** the scope, such that annealing to activate can occur at any time after the dopant region is present (i.e. after the substrate is provided), such that as claimed the 'activation' can occur after the anodizing or oxidizing, which possibilities are not supported or enabled by the original disclosure, hence constitute new matter, such that this claim sequence now further encompasses **New Matter**.

Claim 14 has been broadened in scope, in that now **either** of the **first** or **second** porosity regions may have the **minimum** porosity of about 0.01 %, such that if the second porosity region, which has the lower density, hence higher porosity, has a porosity of about 0.01 % as is claimed to be possible, then the first porosity region **must** have a higher density, thus lower porosity, i.e. a porosity of less than about

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0.01%, which range is not supported by original claim 14. Furthermore, the only disclosure in the specification found to discuss claim values was paragraph [0051], whose teachings were commensurate in scope with original claim 14, **not** amended claim 14, hence as **amended**, claim 14 also encompasses **New Matter**.

With respect to new claim 39, applicants assert (sentence bridging pages 8-9 of 12/6/07 response) support from original claim 38, however independent claim 38 provided an already patterned already porous structure to be oxidized, thus had no limitations concerning when the patterning of a Si-containing substrate was done with respect to forming a dopant region, as it does not even require any dopant regions to exist, let alone when patterning was done with respect to a nonexistent region, nor does it specify whether the structure was porous or not when patterned. The examiner further notes that in applicants' discussed prior art, [0008] follows patterning with a HF-anodization, thus does not relate to forming a dopant region; and while figures 2A-2C, described on [0067+] concerned formation of a pattern structure, there is no patterning prior to forming the dopant region, in fact in figure 2A, activated dopant regions 14, i.e. formation of the dopant regions, appears to be the initiation of patterning. Therefore, as no clear evidence of support has been found or cited for new claim 39, it appears to be **New Matter**.

3. Claims **1-14, 16-24, 26-36 & 39** are rejected under 35 U.S.C. **112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

New clarity issues introduced by the 12/6/2007 amendment to the claims, include in line 6 of claim 1, "that", in the phrase "... region has a lower density than the first porosity region" is nonidiomatic & makes no sense as written, but presumably should be --than--, which is about the only thing that would make sensible phrasing & would be an easy typographical error to make, hence will be so treated for purposes of the rest of the evaluation of the claims on the merits.

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In line 9 of independent claim 1, the claim of "first porosity region coalesces to provide a solid Si-containing overlayer" is of uncertain scope, because all the materials under consideration were already solid, since in order to have the claimed porous regions the "Si-containing substrate" must be solid, as the other possible phases of material, i.e. liquid or gas, are not properly described as porous. Thus, while the claim language implies an intended change, what that change is, is not clear. The examiner notes, if applicants' intent is to alter the first/upper porosity region from being porous to being nonporous, the claims do not necessitate this. However, it must also be noted that since as indicated by original claim 14, applicants consider a material having "a porosity of about 0.01 %..." to be porous, and this corresponds to a material that is about 99.99 % of maximum theoretical density being called 'porous' for purposes of applicants' process, specification & the rejection (although it's doubtful anybody else would consider it porous!), thus almost all materials in existence would be considered porous in light of applicants' specification. Further consider, especially in light of **amended** claim 14, which **now** encompasses porosities of less than about 0.01 % being called porous, that as claimed the second porosity region may have a porosity of 0.01 % (density of 99.99 % of theoretical), thus the first porosity region which is **required** to have a **higher** density, must have a **density** >99.99% theoretical (i.e. 99.991 %, etc.), or **porosity** of <0.01 % (i.e. 0.009, or 0.001, etc.). For these reasons, it is uncertain what the modifier "solid" is intended to supply to the coalescence of the first porosity region in light of applicants' teachings & claim limitations that relate thereto, as this region was already solid.

4. Claims 1-14, 16-24, 26-36 & 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While applicants' amendments have corrected some of the previous 112, second problems noted in section 1 of the rejection mailed 6/15/2007, some remain or have been rearranged, but not completely corrected, as noted below.

Use of relative terms that lack clear metes and bounds in the claims, or in a clear definition provided in the specification or cited relevant prior art, is vague and indefinite. The action of "activated", as now recited in claim 7 for "dopant region", may still be considered a relative term, since the dopant is a generic material, not necessarily ion implanted, where the purpose of the doping is unspecified, as the context of when the annealing to cause the activation, has been removed by the amendment, such that what constitutes activating an unknown dopant for an unknown purpose, at an unspecified time, cannot clearly be determined.

The modifier "neutral" used to describe "neutral ion" in claims 31-34, is also a **relative** term, and while a 'definition' is found in paragraph [0040] that states that the neutral ions do not **interact** with the Si-containing substrate (see section 5 below), that definition **contradicts teachings** in the **same** paragraph, as well as requirements in claims, such as 33, where the neutral ions **interact** by making a region amorphous, thus does not provide a usable or clear definition for what the term "neutral ion" encompasses. Claims 32 & 34, which define the specific "neutral ion" that is used, overcome this problem with respect to what the neutral ion is, but **not** as to what it does. While applicants may be their own lexicographer, if applicants choose to use a term in a manner that is repugnant to its normal usage & the definition they supply is unclear, the terms usage in the claim **cannot** be considered clear or proper. Applicant on pages 9-10 of 12/6/07 response, that "neutral ion" is in reference to having "...no chemical interactions...", but they are supposed definition is not limited to chemical interactions, thus applicant's arguments require one to read limitations into the definition that are not present in the specification, thus essentially demonstrating the examiner's point that the term "neutral ion" & it's definition is unclear.

The examiner notes that "inert gas" is generally not considered a relative term, because it has an art recognized meaning, i.e. is the same thing as a noble gas or a rare gas, in other words the last column of elements in the periodic table, however in applicants' specification in [0043-45], there are given **examples** of inert gas atmospheres and/or oxidizing ambients as "He, Ar, O₂, N₂ and mixtures thereof".

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As this is **not a definition**, it is not binding on the claim language, but this discussion in the specification does shed doubt on the meaning in the claims, which applicant's arguments on page 10 of their response confirmed that the term "inert gas" is intended to be used as a relative term, thus lacks clear metes and bounds (especially considering that with respect to silicon, nitrogen is reactive under some conditions as it may be used to form silicon nitride, thus fitting neither relative meaning of inert, nor periodic table meaning of "inert gas").

The phrasing in claim 34 is a bit awkward, since as written the concluding phrase "at or below nominal room temperature" appears to be associated with "and an implant energy...500 keV", but the examiner assumes due to logic and typical process procedures that the intent is that --said implanting step is performed at or below nominal room temperature using...--, but the meaning in the claim as written still needs to be clear.

5. The disclosure is objected to because of the following informalities: paragraph [0040] has contradictory teachings, as first it teaches that "a neutral ion that **causes damage** formation within the Si-containing substrate 10 is used...", but then it defines the "term 'neutral ions' is used in the present invention to denote any ion that does not **interact** with the Si-containing substrate 10" (emphasis added), however causing damage is a very definite and explicit form of interaction with the silicon-containing substrate, hence these 2 subsequent sentences directly contradict each other. Note that the verb "interact" is a broad term that covers any kind of affect that the "neutral ions" may have on the Si-containing substrate, inclusive of etching, sputtering, chemical reactions, creation of dangling bonds or other disruption of bonds, ionization, heating, momentum transfer, etc., and for there to be no interaction between the two, any "neutral ion" as defined must pass through the substrate without having any effect whatsoever upon the substrate. Note that some subatomic particles, such as neutrinos (which are not ions), are known for not interact with matter except upon rare or infrequent occasions & circumstances, but ions in planting into a substrate can rarely be accurately said to have no interaction therewith.

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Appropriate correction is required.

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-14, 16-24, 26, 35, 29-30 & 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over as **Ikeda Tadashi** (JP 09-064323; also see Patent Abstracts of Japan & 2 machine

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translations), in view of **Hiromitsu** Namita (JP 62-245620, translation supplied & called Hiromitsu Hata et al.).

Applicants have amended the independent claim 1 to include the anodizing from original claim 2, but not the ion implantation therefrom, in required in upper layer of the porous layer to be denser than a lower sub layer of the overall porous reach an, thus removing the 102 over Ikeda, who does not discuss such a porous layer structure per se. However it must be further noted that applicants "porous layer" is in light of the specification & the amendment claim 14, inclusive of materials that no one else would call porous, as they may approach theoretical density of the material.

Ikeda teaches employing a semiconductor substrate, that may be a silicon wafer, which has been doped to be either n-type or p-type, thus reads on having a doped region in the substrate, whether that region is all or part of the substrate. Ikeda also teach treating the n-type or p-type doped with a HF solution, with an exemplary current density of 10-80 mA/cm² creating a porous silicon layer of a desired thickness (~ 100 nm exemplified) via anodization (figures 1 (a-b) & 2 (a-b); [0015-16]; [0022] & [0027]). Note a silicon substrate, with part thereof turned to a porous layer, wherein [0011] of the translations states "forms a porosity layer in the surface [front face] of the [said] semiconductor..." (emphasis added, variation in translations noted) is inclusive of the claimed porosity configuration, but considering the quality of the translations, cannot be considered to necessitate either the claimed configuration, or the previous configuration as set forth in original claim 15. Thereafter, a single crystal silicon layer is deposited over the porous silicon layer, then oxygen ions are implanted through the single crystal silicon layer into the porous silicon layer as part of the oxidation process (an O-containing ambient is clearly present), after which heat treatment is performed at temperatures of 1200-1350°C, so as to form an "embedded oxide film layer" from the ion implanted porous layer, which due to the overall oxidation processing technique is taught to not increase in volume from that of the original porous layer. Options of uniformly ion implanting the porous substrate, or using a patterned resist to mask areas during ion

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implanting, with potentially multiple ion implantings are taught (figures 1 (c-e) & 2 (c-e); [0017-19] & [0022-25]). Ikeda notes that their techniques solve problems discussed with respect to the conventional processes illustrated in figures 3 & 4. With respect to uniformity of buried oxide layer, if one considers the relative meaning of the term, it may be considered covered by Ikeda. If the definition in applicants' specification is considered, the required three layers are present, and while no discussion in Ikeda requires the variation in the buried layers thickness to be less than 20 % of the total buried layer thickness, Ikeda's technique is trying to solve problems of stress & volume expansion beyond the porous layer, so as to not cause **unevenness** of the buried layer ([0010], [0019] & [0025]), such that for continuous buried layers a uniformity within 20% would appear to be encompassed, or alternately it would have been obvious to one of ordinary skill in the art to control processing and as taught so as to prevent unevenness to such a degree as defined, due to the suggestion that unevenness is a problem to be solved. For claimed patterned buried layers, uniformity as defined is impossible, hence cannot be discussed in the context of the definition, but would be considered covered in the context of the relative term.

While Ikeda teaches creating a porous layer (\equiv porous Si-containing region), the percentage of that layer which is porous is not disclosed, nor the distribution of the porosity, however at the claimed range of "about 0.01 % or greater" is so broad that it covers virtually any conceivable amount that may be produced by Ikeda's process & still be called porous. Furthermore, the anodization technique used by Ikeda to create the porosity is essentially the same as the anodization process claimed by applicants & discussed in applicants' specification on [0049-53], as used to convert doped single crystal silicon to porous silicon, thus like porosities would have been expected to have inherently been produced from like processes & materials. Alternately, it would've been obvious to one of ordinary skill in the art to create sufficient porosity in order to effect Ikeda's taught process of creating an embedded or buried oxide layer, where volume increase is not a problem (i.e. avoid crystal & stress defects caused by increased volume during oxidation), such that the compositional parameters, such as degree of doping & the HF anodization

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parameters would have been optimized based on those taught in order to produce required porosity for required effects.

While Ikeda discussed treating a doped (n-type or p-type) silicon substrate, they do not teach particular dopants, the means for effecting the doping, nor require activating the doped region, however it would've been obvious to one of ordinary skill in the art to employ standard n- or p-type dopants & conventional means for silicon wafer doping, which would have been expected to be inclusive of p-type dopants, such as B, in source gases, such as boron fluoride, & conventional means for implanting dopants, such as ion implantation, where ion implantation would have been expected to be especially considered as Ikeda's process is already employing ion implantation techniques, thus equipment therefore would already have been available, providing an economic incentive for employing known ion implanting techniques. Particular ion energies & doses would have been determined by routine experimentation, plus knowledge of the old and well-known process of creating porosity via electrolytic anodization, where required depth, thickness & degree of porosity would have been used in determination of suitable dose and energy, which would in turn affect the distribution of porosity, such that the narrower the energy distribution of the ion beam the be higher the doping concentration in a narrower sub layer of dopant ion implanted layer, which would be known to one of ordinary skill in the art to generally produce higher porosity when anodized. Hence whether density was higher closer to the surface or lower beneath the surface, would have been expected to be related to the depth of the highest implanted dopant concentration, when ion implanting doping techniques were employed. Whether the level or sublayer of highest dopant concentration was nearer or farther from the substrate surface, hence they expected greater or lesser porosity, i.e. inversely lesser or greater density, would have depended on the desired location of the buried oxide layer to be formed, which would have been dependent on the particular device it was intended to be used in. As the need to activate ion implanted dopants is old, well known & would have been known to be necessary in order for the dopants to do their required job with respect to the

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anodization, activating would have been a recognized required step to one of ordinary skill & competence in the art, who would've employed any known & conventional annealing technique and parameters therefore that would have been expected to be effective on the particular semiconductor substrates being employed. Note that as ion implantation to form a layer will inherently cause a gradation of dopant concentrations, due to cross-section effects of ion stopping power for particular energies & materials, thus causing a gradient in the electrical potential with respect to the graded dopant concentration, so the electrolytic anodization process when applied to ion implanted dopant in silicon would have inherently produced a gradation in degree of porosity that varies with respect to the dopant concentration. Note if the implanted ions have an energy optimized for implantation exactly on or at the surface, the concentration best porosity would be greatest at the surface, with both decreasing the further one gets from the surface, while ion implantation optimized for greatest concentration to be below the surface, would have implanted dopant concentration increasing as one approaches the depth optimized for & decreasing at greater depths, with an expected similar effect on porosity when anodized.

The Japanese references to Hiromitsu et al. teach p-type ion implantation into silicon as preparation for creating porous silicon via electrolytic anodization, thus substantiating the above asserted obviousness of employing ion implantation, where Hiromitsu's English abstract is generic with respect to the p-type dopant, but specifically illustrates annealing the ion implanted doped silicon before performing the anodic process in hydrofluoric acid. The translation of Hiromitsu et al. on page 6 indicates B ion implantation (ref. #7) & proton ion implantation (ref. #9, i.e. H⁺), then annealing at 400°C to form an n-type layer under the nitride pattern (ref #5), where porous silicon (ref #11) is formed by anodization in HF, such that areas with greater density (ref #10) are over areas of lower density in a pattern manner.

Thus this secondary reference provides evidence of the known and expected usefulness of ion implantation for creating the required doped regions for electrolytic anodic creation of porous silicon for use in SOI structure formation, as well as the shown desirability of various configurations relating to

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density & porosity, hence illustrating the above discussed obviousness. Also note, that if applicants' claim 31 did not have an impossible definition applied to "neutral ion", the implantation of a proton (H^+) after ion implantation of the p-type dopant in Hiromitsu, might be considered to read on claim 31, as the implantation of hydrogen into the silicon substrate might be considered equivalently interactive as the implantation of Si into the silicon substrate, an element that applicants exemplify as useful as a "neutral ion", but would cause chemical &/or physical interaction in a Si-containing substrate, plus at present it is impossible to define what "neutral ion" might encompass besides the specifically designated elements.

While Ikeda teaches the heat treatment at temperatures of 1200-1350°C encompassed by the claims relevant to claimed oxidizing or "post oxidation step" temperatures, Ikeda does not discuss the atmosphere under which this heat treatment to create the embedded oxide layer is performed, however it would've been obvious to one of ordinary skill in the art to employ atmospheres which either further the oxidation process, prevent contamination during oxidation or the like, such than that as an oxide is being created, it would have been obvious to employ atmospheres that have an oxygen ambient using a common source of oxygen, such as those claimed, where the atmosphere is otherwise unreactive (which obvious logic would suggest to one of ordinary skill in the art use of inert gases to achieve desired pressure, prevent contamination, or like standard purposes), since such would have been expected to prevent out-gassing of oxygen, which would decrease the desired stoichiometry, & since performing oxidations under oxygen atmospheres is a standard procedure. It is noted that use of such an oxygen containing atmosphere during the heat treatment process/annealing would inherently affect the surface of the single crystal silicon layer to affect thermal oxidation thereon, and as such would be further desirable for particular device formation sequences which require such a surface oxide layer. Alternately, the use of the hydrogen ambient would've prevented undesirable reactions with the silicon surface & performing surface passivation thereof, a known desirable effect for many semiconductor device layers.

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8. With respect to Hidekane Ogata (JP 2-164023, translation supplied), as previously discussed, Ogata's English abstract explicitly demonstrates the expected usefulness of ion implanted B for creating a porous structure using fluoric acid electrolytic solution in the anodic formation process & pages 6-7 of the translation discuss ion implantation of the single crystal silicon & anodization in fluoric acid to create porosity with pores over radius of 20-100 Angstroms & density of 40-70%, the showing expected degrees of porosity in terms of the density of the resultant material for analogous processing, however the translation says As, instead of B is used.

As previously noted, background in deSousa et al. (5,188,978; col. 1, line 16-31) was cited for its clear showing that it is old and well-known in the semiconductor art that it is necessary to anneal the semiconductor after ion implantation in order to remove damage caused thereby, so as to appropriately affect or optimize electrical properties and carrier mobility.

9. Claims **1-14, 16-24, 26, 29-30, 35-36 & 38** are rejected under 35 U.S.C. **103(a)** as being unpatentable over Houston et al. (2002/0086463 A1), considering Hiromitsu (JP 62-245620, translation supplied).

Houston et al. teach making an silicon-on-insulator (SOI) wafer, where a first layer of porous silicon is formed by **anodizing a boron** (i.e., p-type) doped silicon wafer using a HF solution, such that **the depth of the porous silicon is controlled** by the timing of the anodization treatment, or by limiting the **depth of the boron doping**, where thicknesses in the range of nanometers to microns can be obtained ([0006]; [0016]). Note, one of ordinary skill would find this a clear suggestion that if presence of dopant is a determinant in the depth of porous microstructure formed, then concentration of that dopant would also be a factor in the amount of porosity formed, thus the resultant density of the porous material at a particular depth. While Houston does not teach the explicit porosity/density configuration of the amended claims with respect to sublayer density, these teachings are inclusive of porosity distributions at the claimed configuration & that of original claim 15, such that it would've been obvious to one of

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ordinary skill in the art how to produce such a configuration & that one of ordinary skill in the art would have expected configurations with different density distributions to be useful in the process & intended enduse.

Houston et al. teach that the anodizing process can result in cracks on the surface of the porous silicon, hence they employ a "prebake" process that fills up surface pores with migrated silicon atoms in order to reduce the surface energy. This "prebake" process seals the surface; may employ a hydrogen ambient; and it may provide a starting point for subsequent epitaxial growth of a layer on the surface, where the quality of the epitaxial layer may depend on the surface pore filling during the sealing bake ([0006]; [0018-19]; [0022]). The epitaxial semiconductor layer may be deposited on the sealed surface either before or after oxygen ion implanting, where the ion implanting may be carried out via plasma oxygen implant or other oxygen implanting methods, with the oxidizing species derived from molecular oxygen or other sources, such as ozone or N_2O , and where oxygen doses may be on the order of 10^{17} - 10^{18} oxygen ions/cm² ([0006]; [0016]; [0020]; [0023-25] & [0031]). The oxidation process, which forms the buried oxide layer from the implanted oxygen is completed by "high-temperature anneal", which appears to use temperatures on the order of 1000°C for about 30 minutes ([0006] & [0020]), but does not specify the atmosphere employed during the anneal, however choices of atmospheres, such as oxygen containing, inert gas containing, H-containing, would have been obvious for reasons as discussed above in section 7, as the process of Houston et al during the post oxygen implantation annealing would have been analogous to those discussed above, especially considering discussion in Houston et al. concerning various oxygen gas sources, as well as H-annealing processing in preceding steps. Houston et al. teach their process provides a number of advantages ([0007-11]), inclusive of aiding a planarity, sharp definition of the oxide layer, etc.

The teachings of Houston et al. differ from the present claims by not discuss as uniform, the buried oxide layer made from the porous layer, its oxygen implantation & anneal thereof, however as

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Houston et al. teach means for controlling the thickness of the porous layer, hence the buried oxide layer, suggesting its thickness measurements can be in the range of nanometers which would be suggestive of a degree of uniformity consistent with that in applicants' specification's definition, and Houston et al.'s layer sequence is consistent with applicants' definition, as it must be applied to the claims if it is employed at all. It would have been obvious to one of ordinary skill in the art that the taught control of depth of the porous layer & contemplated thicknesses for the buried oxide is suggestive of care being taken to create even layers, such that a uniformity of thickness of less than 20% of the layer's thickness would have been well within expected uniformity & reproducibility, especially as the intended use relates to integrated circuit structures where miniaturization, reproducibility, does uniformity can be crucial, and Houston et al. teach advantages of planarity & sharp definition, which are also suggested & supported of uniformity as defined for variation by applicants.

While Houston et al. discusses boron doping to control depths, they do not specify the depth doping performed by ion doping, however such techniques, including activation/annealing of the doped silicon containing substrates, thereafter would have been obvious for reasons as discussed above in section 5, optionally considering secondary references to Hiromitsu [Namita] et al. (JP 62-245620,).

Houston et al. did not provide claimed parameters for current densities for the anodization process nor for the ion implantation process, nor ion beam energies for implantation, nor temperatures for baking/annealing to seal the porous surface in the hydrogen ambient, however given the taught process & objectives of Houston et al., one of ordinary skill in the art would have been expected to employ routine experimentation to determine necessary parameters not explicitly given, such as current densities, energies & temperatures, in order to employ the taught procedure to produce the taught results, which would have been expected to be inclusive of claimed ranges, as no critical differences seen in their effects. Note that Houston et al.'s teaching of the implanting oxygen with plasma or other ion implantation methods, would have been suggestive to one of ordinary skill in the art of oxygen plasmas or

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oxygen ion beams to effect the oxygen implantation, where the parameters of either technique would have been optimized to produce doses on the order claim, noting that in paragraph [0006] Houston et al. teach implantation of low oxygen doses, and that the 10^{18} O ions/cm² is considered to be a relatively heavy dose [0020], which teachings would suggest to one of ordinary skill an apparent preference for the lower end of the taught dosage range.

It is noted that while Houston et al. has much discussion on growing of an epitaxial layer (epi layer), its material is generally not identified, although [0023 & 25] refers to it as an epitaxial semiconductor layer, but [0024] in analogous sequence only refers to a semiconductor layer, not mentioning epitaxial, while [0006] also does not discuss an epitaxial layer in the process sequence, instead discusses forming a thin silicon film by standard deposition techniques on the sealed porous silicon layer, hence growth of an epitaxial silicon layer on the sealed H-prebaked surface is considered taught or suggested by Houston et al., or alternatively obvious due to the overlapping of the teachings for the desired deposit on the sealed surface as presented above.

10. Claims **1-3, 12, 14, 16-24, 26 & 31-36** are rejected under 35 U.S.C. **102(e)** as being anticipated by **or**, in the alternative, under 35 U.S.C. **103(a)** as obvious over **Bendernagel et al.** (6,800,518 B2, which **incorporates** PN 5,930,643 to Sadana et al. by reference).

Claims **4-11, 13 & 39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bendernagel et al.**, optionally in view of **Hiromitsu** Namita (JP 62-245620, translation, as discussed above).

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived

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from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Bendernagel et al. teach forming composite structures, which may include buried insulators (oxides), buried conductive & **buried void plane** structures, by forming a layer of **porous** silicon (or alternately forming vacancies or voids) in the surface region of a semiconductor substrate, such as silicon via electrolytic anodization with a HF-containing solution, where the porosity produced is mainly dependent on the current ($\sim 0.1\text{-}20\text{ mA/cm}^2$) & voltage ($\sim 0.1\text{-}10$ volts typical, $\sim 0.5\text{-}5$ volts preferred) used, the HF concentration, and the **dopant type & concentration** in the wafer, and where thickness of the porous silicon layer may additionally depend on the time ($\sim 30\text{ sec.-}10\text{ min.}$, $\sim 1\text{-}5\text{ min.}$ more highly preferred) of anodization process. Bendernagel et al. particularly note that the thickness of the buried void plane is dependent on device requirements & teach control thereof by adjusting the vertical depth of the porous Si layer formed during the HF-anodization & the dose of the implanted ions (col. 5, lines 33-39). It is particularly specified that "the porous Si layer is typically formed at or below the upper surface region of the semiconductor wafer 10" (col. 6, lines 33-35), thus would have been expected to include density configurations as presently claimed, as well as suggest is obvious configurations consistent with the original claim 15, since in general porosity is inversely related to density. Alternately, given that it is taught that the porous Si layer may be formed below the upper surface of the semiconductor wafer, it would've been obvious to one of ordinary skill in the art to form that porous layer with lesser density than a layer above, which is not taught to be porous, or which may be expected to be less porous due to distribution of dopant atoms which would have been expected to be present for typical doping procedures involving ion implantation.

For this process, Bendernagel et al. teach that the "semiconductor **wafer needs to be doped**, preferably but not necessarily with **p-type** doping atoms. When a **boron**-doped p-type wafer is employed, the dopant concentration of the wafer is typically from about $1\text{E}15$ to about $1\text{E}19\text{ atom/cm}^3$..."

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(emphasis added, col. 6, lines 18-26). Next it is taught that a brief anneal in hydrogen ambient at elevated temperatures may be employed to eliminate open pores on the surface of the porous silicon layer, thereafter an epitaxial silicon (epi-Si) layer on the surface, then the composite substrate is ion implanted, where the ions employed may be oxygen ions, when a buried oxide is intended, or optionally may include nitrogen ions, or just use nitrogen ions for an alternate buried insulator, or metal ions for a buried conductor or void planes. Masking may optionally be employed, with a HF-resistant material (photoresist) before the anodization step &/or a patterned mask for selective ion implantation before implanting, which masks are removed before deposition of the epi-Si or after ion implanting, respectively. Oxygen ion implanting may be in a single or multiple steps, continuous or pulsed, or combined with other ion implantation steps depending on desired structure. Oxygen implanting is taught to be via any conventional ion implantation apparatus, with any conventional ion implanting conditions employed, which are exemplified as O-ion dose from about $1\text{E}16$ - $2\text{E}18$ atoms/cm², implantation energy from about 50 KeV-10 MeV, ion beam current density from about 0.05-500mA/cm², and ion implantation temperature from about 480-650°C. More preferred oxygen ion implantation conditions are also given ($\sim 5\text{E}16$ - $2\text{E}17$ atoms/cm², ~ 150 -300 KeV, ~ 1.0 -10 mA/cm², ~ 550 -600°C) as well as the high-temperature ion implantation step, followed by a normal room temperature ion implantation step exemplified in prior art references. After the ion implanting step(s), high-temperature annealing is performed to transform the implanted oxygen regions into buried oxide regions, while regions that do not contain oxygen ions can be transformed into void layers or buried conductive regions. The high-temperature annealing is performed at temperatures of about 1300°C or greater, but less than the melting point of Si, which is 1415°C, and may be carried out in atmospheres of pure oxygen (O₂), oxygen mixed with an inert gas or N₂, or either without oxygen, or vacuum. When annealing causes significant diffusion of dopants into the overlying silicon layer, a "post" hydrogen annealing process, which may use the same or different conditions (0.25-3 hours, ≤ 82 Torr H-ambient, T = 1100-1150°C), is then employed. Col. 9, lines 7-12

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notes that during annealing, the porous silicon is **consumed** by the formation of the buried oxide/void, and that the epi-Si layer may be thinned by surface oxidation.

Bendernagel et al. teach that the thickness of various layers of the composite structure may vary depending on process conditions employed during fabrication, where typically the buried insulating region has a more highly preferred thickness from about 5-200 nm, and that the thickness of the buried insulating regions is dependent on device requirement and could be **controlled** by adjusting vertical depth of the porous silicon layer form during HF-anodization and the dose of the implanted ions. They are also teaching the possibility of multiple implantations to form different layer structures or side-by-side structures, thus suggesting a reasonable degree of reproducibility or controllability of layer thickness, which would also suggest to one of ordinary skill a similar degree of uniformity where desired, thus for the relative meaning of "uniform", Bendernagel et al. is considered to encompass the claimed "uniform buried oxide layer", or alternately considering the definition of applicants' specification, all the requisite layers are present and given the suggested reproducibility or controllability of the thickness taught for the process, it would've been obvious to one of ordinary skill in the art to control the formation of the buried oxide layer to the degree of providing uniformity as defined, in order to provide layers useful for the types of SOI structures & devices intended to be formed. In the specification of Bendernagel et al., particularly see the abstract; col. 2, lines 58-68; col. 3, lines 20-30 & 40-col. 4, line 44; col. 5, lines 10-15 & 27-39; col. 6, lines 17-col. 10, line 40, especially col. 6, lines 17-col. 7, lines 8 for doping & anodization, col. 7, lines 9-31 for H-anneal to eliminate open surface pores, col. 7, lines 32-44 for the epi-Si layer, typically monocrystalline structure \equiv single crystal, col. 7, lines 45-67 for masking, col. 8 for ion implanting & col. 9 for annealing.

While Bendernagel et al. have extensive discussion of doping, including control of dosage & depth thereof, they do not actually specify ion implantation to effect the doping, however such ion implantation would have been obvious for reasons as discussed above (section

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5), especially in view of the secondary references which provide specific means via ion implantation of providing dopants for analogous processing.

With respect to applicants' claims 31-34, which is directed to "neutral ion" implantation step, Bendernagel et al.'s teachings on col. 8, lines 25-54 might be said to overlap with these implantation steps as they are directed to implantation of atoms besides oxygen & after the doping processing. Specifically, beside suggesting multiple ion implantation steps, implantation of elements, such as nitrogen or metal ions inclusive of Mo, Ta, W, or other refractory metals which have eutectic temperature higher than 1300°C, thus implying that no chemical reaction is occurring, might be consistent with applicants' possible intent of "neutral ions". Furthermore, Bendernagel et al. also suggest looking to other art for ion implantation conditions, such as USPN 5,930,643 by Sadana et al., which was **incorporated-by-reference**, that teaches forming buried oxide layers by creating a damaged buried region in a semiconductor substrate (Si) via ion implantation (O, N, C, Ge, **Bi**, Sb, P, & As), optionally through a capping layer, using a low-dose ion implantation ($\sim \geq 5E16$) at high temperatures about $\geq 200^\circ\text{C}$, plus a **second** yet lower ion dose implantation to form an **amorphous** layer at same or different energies & same or different ions carried out at cryogenic temperatures to about 300°C , at doses of about $2E14$ - $4E15$ ion/cm². The ion implantation in Sadana et al. is followed by an oxidation step typically carried out in an inert ambient (N₂ or Ar) mixed with oxygen at temperatures from about 1300°C or higher, with optional further annealing of the oxidized structure (col. 2, lines 10-43), with col. 7 providing three exemplary sequential treatments, including multiple ion implantation that is followed by a sequence of heating steps at various temperatures, such as initially at 200 - 1000°C in ambient of Ar + 2% oxygen, then at a dozen degrees centigrade in 100% oxygen, followed by 1000 - 1320°C in ambient of 60% Ar + 40% oxygen, followed by further annealing, where temperature is ramped down, thus providing specific parameters for

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specific multistep ion implantation alternatives. All the ions in Sadana et al.'s 2 step or multistep ion implantation process have interactions with the silicon substrate, particularly defect formation or **amorphization**, which while contrary to applicants' definition of "neutral ion" is consistent with the required effect of claim 33 of forming an amorphized region. Also, the specifically suggested ion of Bi, is consistent with applicants' claim of that specific ion, hence these incorporated teachings of Sadana et al. (643) are considered to read on applicants' claims 31-33, with the contradictory nature of their specification taken into account. Furthermore, as an alternative suggested ion is Ge, which is chemically homologous with Si, it is considered that one of ordinary skill in the art would have considered silicon an obvious alternative to this specifically suggested exemplary of ions to be employed in the multi-ion implantation techniques. It will applicant has mostly deleted any necessity for ion implantation of dopants from their claims, Hiromitsu et al. as discussed above, provides further relevant teachings concerning dopants, such as boron for use in porous layer construction via anodization, which are relevant to Bendernagel et al.

11. Claims **1-14, 16 24, 26, 31-36 & 39** rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14-38 of U.S. Patent No. **6,800,518 B2** (Bendernagel et al.), **optionally** in view of **Sadana et al.** (5,930,643) & optionally in view of **Hiromitsu et al.** (JP).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the Bendernagel et al. claims are directed to the same basic step with overlapping limitations with respect to details, such as parameters, patterning or lack thereof (note that one may selectively implant an area predetermined to be the entire surface, i.e. blanket implantation), order in which specific limitations are emphasized, all of which may be considered obvious variations on the same theme. Note in claims 14

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& 38, the formation of a porous Si layer in a surface region, is inclusive of one with the claimed density distribution. For instance, the patent to Bendernagel et al. claims forming a porous silicon layer in a surface region using parameters that overlap with claim parameters, thus while the specific porosity ranges or distributions of claims 14 or 15 are not claimed in the patent, due to the almost all-encompassing breath of about 0.1 % or greater porosity in claim 14 & the overlapping electrolytic anodization parameters, the presently claimed porosity range would have been expected to significantly overlap with expected effects of the patented procedure. Optionally, it would alternately have been obvious to one of ordinary skill in the art to use procedures such as in the claims of Bendernagel et al. to form device structures as set forth in Hiromitsu, which would have involved patterning procedures that produced distributions of density has claimed.

With respect to dependent claims 2-3, which require a silicon-containing (i.e. as defined on p.6, [0026] "a semiconductor material that includes at least silicon") substrate, which is doped (n-type or p-type) dopant, the claims in the Bendernagel et al. patent do not mention whether the semiconductor (Si) substrate is doped, however read in light of Bendernagel et al.'s specification, the substrate must be doped in order to perform the claimed electrolytic anodization (col. 6, lines 18-26 & 45-52; col. 7, lines 1-8; & col. 9, lines 41-45), thus n-type or p-type doping is considered to be compassed.

The patent claims also are not directed to uniformity of buried oxide, or layer distribution (, or thickness), however as they are directed to a composite semiconductor structure expected to be used for finely patterned devices, one of ordinary skill in the art would have expected to produce layer thicknesses typically desirable for such semiconductor devices which would have been expected to have the same degree of uniformity, especially given a lack of significantly different critical procedures, and for that uniformity to be sufficient for taught end uses or devices.

While the patent claims include oxygen ion implantation parameters of dose, implantation energy & ion beam current, as well as repeating the step of oxygen ion implant any number of times which

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overlaps with presently claimed oxygen ion implantation, including two oxygen implantation steps; the patented claims are not directed to the specific parameter of temperature during single or multiple oxygen ion implantations, however it would have been obvious to one of ordinary skill in the art to employ conventional temperatures for ion beam implantation, which would have been expected to encompass claimed temperature ranges, where choice of temperature would have been expected to be dependent on particular desired structure formation consistent with production of the claimed varied layers, thus expected to encompass claimed temperatures & employ different temperatures when the effects of the two steps are intended to be differentiated, as temperature is old and well known to affect resultant microstructure. Optionally, claimed temperatures for two oxygen ion implantations would have been further obvious in view of Sadana et al. (discussed above in section 9), who is also directed to creating buried oxide regions in semiconductors via oxygen ion implantation, where the desirability of providing two different effects (buried damage region & adjacent amorphous layer) via use of two ion implantations differentiated by dosage & temperature, is taught for controlling resultant oxide thickness & properties (col. 2, lines 1-43+; col. 4, lines 7-29 for first ion implantation & lines 30-65 for second ion implantation; col. 6, lines 8-16 note that the defect containing amorphous region is believed to enhance oxygen diffusion into the silicon & combine with the first created damage layer during the annealing step to form the buried oxide region; figure 2 & col. 6, lines 47-59 this 2-step, 2 temperature ion implantation taught to improve electrical & structural qualities of oxide layer & save implant time & wafer cost), hence it would've been further obvious to one of ordinary skill in the art given the claimed parameters & claimed multiple ion implantations, to employ a known technique as discussed in Sadana et al. for its taught advantages in producing analogous buried oxide layers using analogous ion implantation with analogous subsequent annealing techniques, with the expectation that advantages taught in Sadana et al. would also be relevant to Bendernagel et al.'s patented process. Also note below discussion concerning obviousness of uniformity in buried oxide regions with respect to Sadana et al.'s .

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12. As the anodization step has been included in the independent claimed, the rejections based on **Sadana et al.** (5,930,643), & Norcott et al. (6,486,037 B2) have been overcome, as the defect regions created therein are not subjected to anodization.

As previously noted, Sadana et al. (6,222,253 B1) was cited as substantially equivalent to Sadana et al. (643), for purposes of the rejection, except that it only discusses the two-step ion implantation sequences, with analogous subsequent annealing steps, rather than also discussing the option multiple lower temperature & dose oxygen ion implantations subsequent to the initial oxygen ion implantation (summary, especially col. 2, lines 49-col. 3, lines 7; & col. 4, line 10-col. 5, lines 37). However, it is particularly noted that Sadana et al. (253) substantiates the above arguments of including "vacancies" as types of defects created in the initial oxygen ion implantation step, since in col. 4, lines 40-49 oxygen ion implantations in doses of $(3-5)10^{17}$ ion/cm² are explicitly taught to cause "Si damage clusters of Si atoms, Si in interstitial locations and Si vacancies with and/or without oxygen", which can be considered microstructural voids.

Roitman et al. (6204546 B1: abstract; summary; col. 2, lines 44-col. 4, lines 24) has substantially equivalent disclosure to Sadana et al. ((253) or (643)) for purposes of the rejection, except is more similar to (253) & teaches at the first ion implantation creates "silicon crystal and defect regions having stacking faults and dislocation defects" (col. 2, lines 56-57), where dislocation is considered to be substantially equivalent to vacancies, and discusses buried oxide layer thicknesses in the range of 300-800 Angstroms (i.e. 30-80 nm).

13. Claims 1--14, 18-24, 26-28, 31--36 & 39 are rejected under 35 U.S.C. 102. 103(a) as obvious over Hodge et al. (5,387,541), in view of Hiromitsu et al. for reasons as discussed above.

Hodge et al. teach various possible routes for creating a porous layer within the silicon substrate, which may be oxidized so as to form a buried silicon layer. Specifically see the abstract; figures, noting figure 1 is a flow diagram suggesting various process routes, figure 2 illustrates blanket treatment, while

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figures 3 & 4 illustrate pattern treatments; col. 1 discusses known prior art porosity treatments, teaching that dopant level determines number & size of pores (col. 1, lines 8-17), with discussion of porosity levels, such as less than 50% (col. 1, lines 37); paragraph bridging cols. 1-2 discusses the importance of eliminating nonuniformity; col. 2, lines 14-29 sets forth the basic process sequence of manufacturing a porous silicon layer in the silicon wafer, then ion implanting into the porous layer causing amorphization therein, followed by recrystallization/annealing; col. 2 lines 36-68 & col. 5, lines 30-48 discussed electrolytic anodization using hydrofluoric acid (HF), with an exemplary current density of 5.5 mA/cm^2 ; col. 3, lines 1-3 teaching "pre-anodization p⁺ implant of the non-porous silicon surface and annealed in order to enhance uniformity of current flow through the wafer during anodization", which is considered to read on ion implanting a dopant, activation thereof by annealing, plus inherently creating a gradient effect in the porosity since ion doping will create a gradient concentration of dopant; col. 3, lines 4-53 & col. 5, lines 49-col. 6, lines 3 ion implantation after annealing may include ions, such as Ge⁺, Si⁺, Sn⁺, etc., where amorphous layer is produced & multiple ion implantations may be employed, with lines 44-54 noting optional use of masking to create amorphous silicon islands on porous silicon surface; col. 3, lines 58-64 & col. 6, lines 4-17 discussing typical annealing procedures, including preferred alternatives of 3 minutes rapid thermal annealing at 950°C in Ar and also 24 hours at 525°C in nitrogen or argon; col. 3, lines 65-col. 4, line 53 & col. 6, lines 56-col. 7, line 20 for various oxidizing procedures that may be employed when SOI material is desired to be produced, including possible patterning (col. 4, lines 10-19), a stabilizing oxidation process annealing at 300°C for an hour in flowing oxygen (col. 4, lines 20-31), a wet oxidation process that uses various sequences or temperatures, including wet oxidation at 800°C for two hours, followed by 1090°C wet oxidation four minutes, where wet oxidation may typically include gases of H₂ & O₂ (col. 4, lines 32-54).

Hodge et al. does not explicitly state that the buried oxide layer, which they may produce, is "uniform" nor provide a degree of uniform as in applicants' specification definition, however as the same

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process steps as claimed are employed, the resultant effect would have been expected to be of analogous uniformity, whether one considers that term as a relative term, or within the scope of applicants' 20% thickness uniformity, as combined with defined upper & lower layers which are consistent with the results of Hodge et al., especially considering their teachings on enhancing uniformity of current flow during anodization, which would have been expected to enhance uniformity of porous layer formation, thus uniformity of resultant buried layer formed therefrom. Alternately, it would've been obvious to one of ordinary skill in the art to employ the taught process for making SOI structures so as to make sufficiently uniform, reproducible layers useful for semiconductor device formation. Also see above analogous discussions.

Above discussions concerning doping, ion implantation distribution & reasons for distribution in configurations as claimed also applied Hodge et al., especially in view of Hiromitsu et al. for reasons as discussed above. As previously discussed, dependent claims differ by requiring specific dopants, such as B, instead of generic teachings of the patent & specific parameters for the implantation, by claiming alternative variations on the activation/annealing process after implantation, including the art gas used in the oxygen ambient for oxidizing, specifically claiming repeating the process to create multilayered results, and claiming specific ion implantation parameters for the choice of Si ion as the "neutral ion", however these are all obvious variations relevant to routine experimentation & optimization of the process as taught by Hodge et al. and would not be considered to provide patentable significance to the process, as such routine experimentation considerations of the teachings of Hodge et al. would have been expected to encompass such parameters given their teachings that produce analogous results from otherwise like steps. Alternately, with respect to claims 4-6 which are directed to specific dopants including the p-type dopant B, Hodge et al. suggest p-type ion implantation in general for the creation of the porous layer, where Ogata et al. provide the specific usefulness of boron for this purpose, thus substantiating the above

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asserted obviousness, as one of ordinary skill the art would have looked to analogous prior or such as about that at how to determine expected effective p-type dopants that may be on an implanted.

14. While Blewer et al. (5,023,200) includes teachings on anodization it does not include teachings that necessitate the claimed configuration, but remains of interest to the claims & may be considered cumulative for its teaching concerning multilayers, anodization, etc..

In Blewer et al., see the abstract; figures; col. 1, lines 65-col. 2, lines 10 (note teachings on uniformity of porous silicon layer, but no specific % values), 29-44 & 59-66; and col. 3, lines 30-col. 4, lines 32; col. 6, lines 13-68, especially 59-68 where the exemplary "about 10 mA for 100 mm wafer diameter" gives a value of 0.064 mA/cm²; & claims especially 12-14. Blewer et al. specifically notes the known importance of uniformity in a buried oxide layer, however does not teach % values as defined in applicants' specification, however for this process with no critically different processing steps, like values will inherently have been encompassed. Also see above discussions on obviousness of producing uniformity.

15. As previously discussed, References of Aspar et al. (6808967 B1), D'Arrigo et al. (6506658 B2) & Lin (7067387) contain analogous teachings to those discussed in above references, however are redundant for the claims as presently written. Sato et al. (5854123) is cited as of interest, as relating to analogous process employing electrolytic anodization for creating porosity, also discussing ion implantation & oxidation steps.

16. Applicant's arguments filed 12/6/2007 & discussed the have been fully considered but they are not persuasive.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 8:30 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Marianne L. Padgett/
Primary Examiner, Art Unit 1792

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